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In the claims:

For the Examiner's convenience, all pending claims are presented below with changes shown.

1. (Currently Amended) An apparatus, comprising:

a first interface;

a second interface not directly coupled to said first interface; and

a cache accessible from said first interface and said second interface, to contain a cache line, the cache line ~~simultaneously~~ having ~~two~~ a joint cache coherency states ~~with~~ wherein the cache line has a first cache coherency state when accessed from said first interface and a second cache coherency state when accessed from said second interface, wherein said first cache coherency state has higher privilege than said second cache coherency state when said second interface is coupled to a processor.

2. (Cancelled)

3. (Previously Presented) The apparatus of claim 1, wherein said second cache coherency state is to reduce snoop transactions on said second interface.

4. (Previously Presented) The apparatus of claim 1, wherein said first cache coherency state is exclusive and said second cache coherency state is shared.

5. (Previously Presented) The apparatus of claim 1, wherein said first cache coherency state is modified and said second cache coherency state is shared.

6. (Original) The apparatus of claim 3, wherein said second cache coherency state supports speculative invalidation.

7. (Original) The apparatus of claim 6, wherein said first cache coherency state is modified and said second cache coherency state is invalid.

8. (Original) The apparatus of claim 6, wherein said first cache coherency state is exclusive and said second cache coherency state is invalid.

9. (Original) The apparatus of claim 6, wherein said first cache coherency state is shared and said second cache coherency state is invalid.

10. (Original) The apparatus of claim 6, wherein said second cache coherency state further supports explicit invalidation.

11. (Previously Presented) A method, comprising:

associating a first cache coherency state with a first cache line in a first cache, said first cache coherency state being a single cache coherency state, said first cache coupled to a first interface and to a second interface;

associating a second cache coherency state with a second cache line in a second cache coupled to said first cache via said second interface;

transitioning said first cache coherency state to a joint cache coherency state including said first cache coherency state for said first interface and a third cache coherency state for said second interface; and

transitioning said second cache coherency state to said third cache coherency state.

12. (Original) The method of claim 11, wherein said first cache coherency state is exclusive, said second cache coherency state is invalid, and said third cache coherency state is shared.

13. (Original) The method of claim 11, wherein said first cache coherency state is modified, said second cache coherency state is modified, and said third cache coherency state is invalid.

14. (Previously Presented) A method, comprising:

associating a first cache coherency state with a first cache line in a first cache, said first cache coherency state being a single cache coherency state, said first cache coupled to a first interface and to a second interface;

associating a second cache coherency state with a second cache line in a second cache coupled to said first cache via said second interface;

transitioning said second cache coherency state to an invalid state; and

transitioning said first cache coherency state to a joint cache coherency state including said first cache coherency state for said first interface and an invalid state for said second interface.

15. (Original) The method of claim 14, wherein said first cache coherency state is modified.

16. (Original) The method of claim 14, wherein said first cache coherency state is exclusive.

17. (Original) The method of claim 14, wherein said first cache coherency state is shared.

18. (Previously Presented) A method, comprising:

associating a first cache coherency state with a first cache line in a first cache, said first cache coherency state being a single cache coherency state, said first cache coupled to a first interface and to a second interface;

associating an invalid state with a second cache line in a second cache coupled to said first cache via said second interface;

transitioning said invalid state to a shared state; and

transitioning said first cache coherency state to a joint cache coherency state including a shared state for said second interface.

19. (Original) The method of claim 18, wherein said first cache coherency state is invalid and said joint cache coherency state is exclusive-shared.

20. (Original) The method of claim 18, wherein said first cache coherency state is modified-invalid and said joint cache coherency state is modified-shared.

21. (Previously Presented) An apparatus, comprising:

means for associating a first cache coherency state with a first cache line in a first cache, said first cache coherency state being a single cache coherency state, said first cache coupled to a first interface and to a second interface;

means for associating a second cache coherency state with a second cache line in a second cache coupled to said first cache via said second interface;

means for transitioning said first cache coherency state to a joint cache coherency state including said first cache coherency state for said first interface and a third cache coherency state for said second interface; and

means for transitioning said second cache coherency state to said third cache coherency state.

22. (Original) The apparatus of claim 21, wherein said first cache coherency state is exclusive, said second cache coherency state is invalid, and said third cache coherency state is shared.

23. (Original) The apparatus of claim 21, wherein said first cache coherency state is modified, said second cache coherency state is modified, and said third cache coherency state is invalid.

24. (Previously Presented) An apparatus, comprising:

means for associating a first cache coherency state with a first cache line in a first cache, said first cache coherency state being a single cache coherency state, said first cache coupled to a first interface and to a second interface;

means for associating a second cache coherency state with a second cache line in a second cache coupled to said first cache via said second interface;

means for transitioning said second cache coherency state to an invalid state; and

means for transitioning said first cache coherency state to a joint cache coherency state including said first cache coherency state for said first interface and an invalid state for said second interface.

25. (Previously Presented) The apparatus of claim 24, wherein said first cache coherency state is modified.

26. (Previously Presented) The apparatus of claim 24, wherein said first cache coherency state is exclusive.

27. (Previously Presented) The apparatus of claim 24, wherein said first cache coherency state is shared.

28. (Previously Presented) An apparatus, comprising:

means for associating a first cache coherency state with a first cache line in a first cache, said first cache coherency state being a single cache coherency state, said first cache coupled to a first interface and to a second interface;

means for associating an invalid state with a second cache line in a second cache coupled to said first cache via said second interface;

means for transitioning said invalid state to a shared state; and

means for transitioning said first cache coherency state to a joint cache coherency state including a shared state for said second interface.

29. (Original) The apparatus of claim 28, wherein said first cache coherency state is invalid and said joint cache coherency state is exclusive-shared.

30. (Original) The apparatus of claim 28, wherein said first cache coherency state is modified-invalid and said joint cache coherency state is modified-shared.

31. (Currently Amended) A system, comprising:

a cache accessible from a first interface and a second interface, to contain a cache line, the cache line ~~simultaneously~~ having ~~two~~ a joint cache coherency states ~~with~~ wherein the cache line has a first cache coherency state when accessed from said first interface and a second cache coherency state when accessed from said second interface, wherein said first cache coherency state has higher privilege than said second cache coherency state when said second interface is coupled to a processor;

a bus bridge to a third interface; and

an input-output device coupled to said third interface.

32. (Cancelled)

33. (Original) The system of claim 31, wherein said second cache coherency state is to reduce snoop transactions on said second interface.